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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,993	09/17/2003	Yukio Sugimura	56937-091	1975

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EXAMINER	
GENTRY, DAVID G	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,993	SUGIMURA ET AL.	
	Examiner	Art Unit	
	David G. Gentry	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Udell, Jr. (U.S. Patent No. 5,291,495) in view of Chrudimsky et al. (U.S. Patent No. 6,745,357).

As per claim 1, Udell discloses a technique for testability of a semiconductor integrated circuit, comprising:

the first step of conducting a fault simulation for the semiconductor integrated circuit based on a predetermined test pattern and discriminating a detectable fault and an undetectable fault from each other (column 2, line 65- column 3, line 2);

the second step of list undetectable faults as undetected faults (column 4, lines 6-9);

the third step of determining the test conditions for testing the undetected faults (column 4, line 63- column 5, line 4);

the fourth step of determining a test pattern most likely to meet the test conditions of the third step from among predetermined test patterns of the fault simulation of the first step (column 4, line 63- column 5, line 4; Note: the test pattern is found by determining a test that will make all faults observable);

the fifth step of replacing registers associated with the undetected faults of the second step with scan circuits and connecting the scan circuits in a scan chain thereby to construct a modified circuit (column 5, lines 4-8); and

the sixth step of conducting the fault simulation or the test by switching to the test condition determined in the third step at the timing corresponding to the undetected faults while using the determined test pattern in the fourth step for the modified circuit (column 5, lines 8-17).

Udell fails to disclose a scan test method using registers, but he instead describes using flip-flops.

Chrudimsky discloses a scan test using scan registers (column 1, lines 23-58).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the method using scan registers as described by Chrudimsky in the method described by Udell. It would have been obvious because it allows the registers that are deeply imbedded in the integrated circuit to be tested (column 1, lines 30-32).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Udell and Chrudimsky in further view of Maeno (U.S. Patent No. 6,678,846).

Udell and Chrudimsky are relied upon for reasons stated in the previous section.

Udell and Chrudimsky fail to disclose a technique for testability of a semiconductor integrated circuit wherein the input registers associated with undetected faults are replaced by registers with set or reset function.

Maeno discloses a technique for testability of a semiconductor integrated circuit wherein the fifth step includes the step of replacing the input-side registers associated with the undetected faults not by scan registers but by registers with set or reset function thereby to constitute a modified circuit (column 14, line 59- column 15, line 13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the input registers with set or reset function as described by Maeno in the method described by Udell and Chrudimsky. It would have been obvious because it allows the circuit to be reset by outside signals (column 15, lines 7-13).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Udell in view of Huang et al. (U.S. Patent No. 6,415,403), Golshan (U.S. Patent No. 6,219,812) and Chrudimsky.

Udell discloses a technique for testability of a semiconductor integrated circuit, wherein the registers connected to a combination logic circuit constituting an object of the test in the semiconductor integrated circuit are classified into first registers that can be controlled and observed directly from a built-in processor, second registers that can be controlled and observed directly from a terminal of the semiconductor integrated circuit and third registers other than the first and second registers, the technique comprising:

the first step of replacing the third registers with scan registers and connecting the scan registers in a scan chain to thereby constitute a modified circuit (column 5, lines 4-8);

the third step of setting and inputting the test data to the third register with the shift operation through the scan chain (column 5, lines 8-17);

the fourth step of performing the capture operation of the test data for the combination logic circuit (column 1, lines 45-54; Note: Udell is using a scan path which is used to capture test data and output it);

the fifth step of outputting the test result data from the third register with the shift operation through the scan chain (column 1, lines 45-54; Note: Udell is using a scan path which is used to capture test data and output it); and

Udell fails to disclose a first set of registers connected directly to a processor or a second set of registers connected directly to the integrated circuit terminal.

Huang discloses a technique for testability of a semiconductor integrated circuit, wherein the registers connected to a combination logic circuit constituting an object of the test in the semiconductor integrated circuit are classified into first registers that can be controlled and observed directly from a built-in processor (column 2, lines 56-64; the BIST controller represents the processor), the technique comprising:

the second step of setting and inputting the test data to the first registers from the processor (column 2, lines 56-64); and

the sixth step of outputting the test result data from the first registers (column 2, lines 56-64).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the registers connected to the processor as described by Huang in the method described by Udell. It would have been obvious because this input technique allows for test patterns to be input into the scan chains (column 2, lines 56-64).

Udell and Huang fail to disclose a set of registers connected directly to an integrated circuit terminal.

Golshan discloses a technique for testability of a semiconductor integrated circuit, wherein the registers connected to a combination logic circuit constituting an object of the test in the semiconductor integrated circuit are classified into second registers that can be controlled and observed directly from a terminal of the semiconductor integrated circuit (column 1, lines 29-45; the semiconductor terminal is what is scanning in the test patterns), the technique comprising:

the second step of setting and inputting the test data to the second registers from the integrated circuit terminal (column 1, lines 29-45); and

the sixth step of outputting the test result data from the second registers (column 1, lines 29-45).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the registers connected to the semiconductor terminal as described by Golshan in the method described by Udell and Huang. It would have been obvious because this scanning-in technique allows for testing the interconnections between integrated circuits (column 1, lines 29-45).

Udell fails to disclose a scan test method using registers, but he instead describes using flip-flops.

Chrudimsky discloses a scan test using scan registers (column 1, lines 23-58).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the method using scan registers as described by Chrudimsky in the method described by Udell. It would have been obvious because it allows the registers that are deeply imbedded in the integrated circuit to be tested (column 1, lines 30-32).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Gentry whose telephone number is (571) 272-2570. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER